Amendments to the Drawings

Please substitute the attached two sheets of replacement formal drawings, containing Figs. 1-4 for the current drawings

REMARKS

The Office Action of December 31, 2007, and the references cited therein have been carefully considered.

In this Amendment, the specification has been amended to provide proper section headings as suggested by the Examiner, corrected formal drawings have been filed and the claims have been amended only to overcome the Examiner's formal objections and rejections and to correct noted informalities. Finally, a new independent claim 6, which is similar to claim 1 but more specifically defines the switching circuit, with dependent claim 7 have been added.

As indicated, new corrected formal drawings have been filed as required by the Examiner. It is requested that the Examiner acknowledge receipt and acceptance of the new formal drawings in the next Office Action.

In view of the amendments to the specification and line 1 of claim 1, it is submitted that the Examiner's formal objections to the specification and claim 1 have been overcome and should be withdrawn.

Reconsideration of the rejection of claims 1-5 under 35 U.S.C. §112, second paragraph, as being indefinite is respectfully requested. Although applicant is of the opinion that both of the terms objected to by the Examiner are terms well understood by those skilled in the art to which the present invention pertains, claim 1 has been amended to delete the term "very low ohmic resistance" since the inductive element with this property is structurally defined in the claim as simply a conductor of predetermined length and the specification provides support for the desired ohmic value. However, it is submitted that the objection to the term "high-frequency ferrite" is not well founded as this term is well known and commonly used in the electronics art. In this regard, the Examiner is referred to the Pomponia reference applied in rejecting the claims of the present application. Throughout this patent, reference is made to high-frequency and low-frequency ferrites, e.g., column 2, lines 38-50; column 3, lines 45-50; and the first two claimed elements of claim 1, i.e., the core bodies. The difference between low

frequency ferrites and high- frequency ferrites is that low frequency ferrites have increased eddy current losses above 50-100 kHz while high frequency ferrites have low eddy current losses until a much higher frequency range. This is well known to those skilled in the art and is consistent with the teachings of the Pomponia patent. Accordingly, it is submitted that the term "high-frequency ferrite" is not indefinite and thus that claim 1 as now amended fully complies with 35 U.S.C. §112, second paragraph.

The rejection of claims 1-5 under 35 U.S.C. §103(a) as being unpatentable over the patent to Choi in view of the patent to Pomponio has been noted and is respectfully traversed. In urging this ground of rejection, the examiner has essentially taken the position that the Choi patent discloses all of the claimed features except for the inductive element constituted by a conductor of predetermined length; that such an inductive element is taught by the Pomponio patent; and that consequently, it would be obvious to substitute the inductive element of Pomponio for the inductive element of Choi and arrive at applicants claimed invention. It is submitted, however, that even if it was obvious to combine the teachings of the two references in the manner suggested by the Examiner, the resulting arrangement would not be the invention as defined in claim 1.

The present invention as defined in claim 1 is directed to a circuit for switching or connecting two high capacity condensers in parallel. As described in the background portion of the application, and as shown in the Hungarian patent application mentioned on page 1, line 14, of the present application, which Hungarian application corresponds to U.S. Patent No. 6,479,969 (of record in the present application), high transient currents flow when a second condenser is connected in parallel with a high voltage. Unless protection is provided, such high transient currents may destroy the condensers and the switch. The present invention seeks to prevent the destruction of the condensers and the switch during the transient process but to use as little delay as possible in order not to slow down or distort the main voltage waveforms through the condensers. Thus the

invention provides for a very short delay for the switching transistor caused by the RC delay member or circuit in the control circuit for the switching transistor and a further independent delay by the inductance in the main circuit of the switching transistor that prevents the flow of a current that is too high through the FET transistor before it reaches its fully open state. That is, the prevention time is the transient period within which the transistor changes from a high impedance state to a low impedance state. The inductance is realized by the simple conductor of predetermined length surrounded by a ferrite core. Such an arrangement, with or without the specific inductance is found in the Choi patent.

The Choi patent is not concerned with switching or connecting two condensers in parallel and is not concerned with the problem of suppressing large transient currents to protect the components. The circuit of Choi is for correcting the power factor of a signal and uses a completely different circuit arrangement. Initially the two condenses are not connected in parallel at any time. Moreover, the RC delay element for the transistor 12, which the Examiner considers to be the resistor Rf and the capacitor Cf are not connected between the gate electrode of the transistor 12 and the control input of the transistor. Rather the RC member Rf, Cf of Choi is connected in the source circuit of the transistor 12. In this circuit, the voltage on the capacitor Cf follows the voltage drop on resistor Rcs in the manner of a conventional emitter (source) follower circuit, and produces the typical output signal Vcs of the transistor 12, which signal is then used for feedback control. In the Choi circuit, the control gate of the transistor 12 is connected directly to the output of drive circuit 54. Any delay caused by the RC member Rf, Cf of Choi has no effect on the speed with which transistor 12 switches between open and closed states. Moreover, the transistor 12 does not the function of interconnecting or switching the capacitors C1 and C0 in parallel, since the filter element L and the diode D1 are connected between the two capacitors , and thus would prevent high currents from flowing between the two capacitors. Finally, the waveforms of Figs. 8 and 9 indicate that there are reversed sawtooth waveforms involved, where there

is no sudden rises in voltage. As a result, there is no mention of transient energy problems concerning the load on the FET transistor 12 and consequently no teaching of providing two separate delays to deal with such transient voltages as recited in claim 1. Accordingly, for the above stated reasons, it is submitted that claim 1 patentably distinguishes over the Choi patent even if it were provided with an inductive element as taught by Pomponio.

It should also be noted that the Pomponio device is a noise suppression circuit for broad band applications based on the juxtaposition of a high frequency ferrite and a low frequency ferrite. There is no mention in this patent about any delay effect of the described structure or that the described element should be used as an inductive element in a high power electronic switch. Accordingly, it is submitted that one skilled in the art would not consider substituting the device of Pomponio for the inductance L of Choi except through the use of hindsight in an attempt to arrive at the invention defined in the claims. Accordingly, for these additional reasons, it is submitted that claim 1 is allowable over the combination of the Choi and Pomponio patents.

Claims 2-5 are dependent on claim 1 and are allowable over the Choi-Pomponio combination of references for at least the same reason as claim 1. Note further that the capacitance Cf of Choi has nothing to do with the input capacity of the field effect transistor 12 of Choi since it is not in the input circuit of the transistor (claim 4).

Newly presented claim 6 contains substantially all of the limitations of claim 1 but more specifically defines the connections between the two condensers, the switch and the RC delay network. This circuit arrangement is clearly not found in the circuit of Choi. Accordingly, for these reasons as well as those discussed above with regard to claim 1, it is submitted that claim 6 and claim 7 dependent thereon are allowable over the combination of the Choi and Pomponio patents.

In view of the above amendment, and for the above stated reasons, it is submitted that all of the pending claims, i.e., claims 1-7, are allowable over the prior art of record and are in condition for allowance. Such action and the passing of this application to issue are therefore respectfully requested.

If the Examiner is of the opinion that the prosecution of this application would be advanced by a personal interview, the Examiner is invited to telephone undersigned counsel to arrange for such an interview.

Respectfully submitted,

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